May 23, 2024

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ELEC4712: Thesis A

Formally Verifying a Block MiniFloat Multiplier Accumulator Unit

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# Introduction

## Purpose

The primary focus of my thesis is the formal verification of an alternative computing representation of fractional numbers called Block MiniFloat, an 8-bit floating point number. This research aims to thoroughly understand and validate the basic mathematical properties and computational behaviour of Block MiniFloat to ensure its reliability and precision in various applications.

The importance of this research lies in the need for efficient and accurate fractional number representations in computing. All traditional floating-point representations, such as 64-bit, 32-bit, and 16-bit as defined by the IEEE 754 standard, have inherent limits to their precision and are susceptible to rounding errors. By investigating these traditional representations, we have moved towards a parallel method to verifying Block MiniFloat.

The primary objectives of this thesis are:

1. To analyse and verify the mathematical properties of floating-point addition.
   1. Commutativity
   2. Associativity
   3. Special Case handling.
   4. Overflow / Underflow
2. Extend this to Subtraction
3. Extend this to multiplication.
4. To compare its precision and efficiency with traditional floating-point representations.

## Background

# Literature Survey

## Key Themes

### Topic 1

### Topic 2

### Topic 3

## Gaps in the Literature

# Thesis Progress

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