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ELEC4712: Thesis A

Formally Verifying a Block MiniFloat Multiplier Accumulator Unit

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# Introduction

## Purpose

The primary focus of my thesis is the formal verification of an alternative computing representation of fractional numbers called Block MiniFloat, which is an 8-bit floating point number. This research aims to thoroughly understand and validate the mathematical properties and computational behaviour of Block MiniFloat to ensure its reliability and precision in various applications.

The importance of this research lies in the need for efficient and accurate fractional number representations in computing. All traditional floating-point representations, such as 64-bit, 32-bit, and 16-bit as defined by the IEEE 754 standard, have inherent limits to their precision and are susceptible to rounding errors. By investigating these traditional representations, I have gained a comprehensive understanding of their precision limits and the methods used to mitigate rounding errors, such as multiple versions of rounding and expanding operations away from complex functions like logarithms.

The primary objectives of this thesis are:

1. To analyse and verify the mathematical and computational properties of the Block MiniFloat representation.
2. To compare its precision and efficiency with traditional floating-point representations.
3. To identify potential applications where Block MiniFloat can be effectively utilized.
4. To develop and implement verification methods to ensure the accuracy and reliability of Block MiniFloat in practical computing scenarios.

## Background

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